column 6, lines 14-22, and "selecting between standard fast page mode (non-EDO) and burst mode" at column 7, lines 44-55. These portions of Manning are insufficient to disclose the subject matter of the claims 22-32 and 59.

Applicant believes that the Office misapprehends the Manning reference, and applicant would like to clarify. Applicant has explained that EDO mode is a mode that provides a longer period of time for when data is valid at the outputs of a DRAM. *See* applicant's specification at page 3, lines 19-21. Applicant has discussed that fast page mode is a mode that uses a row address strobe to latch a row address portion of a DRAM address. *See* applicant's specification at page 2, lines 12-13. Applicant has also explained that pipelined mode is a mode that divides address information into operational times such that the address information can be provided from an external source as a stream of data. *See* applicant's specification at page 8, lines 1-13.

The Office indicated that "Manning discloses switching between fast page pipeline and burst pipeline." First, applicant is unclear about what is a fast page pipeline or a burst pipeline; applicant cannot find them in Manning. Second, the Office is correct in that Manning indicated that "[t]he current invention include[s] a pipelined architecture." See Manning at column 5, lines 43-44. But this should be read in the context of Manning's Field of the Invention: "This invention relates more specifically to circuits and methods for controlling memory write cycles in burst access memory devices." See Manning at column 1, lines 11-13. Compare to the applicant's Field of the Invention: "This invention relates ... more particularly to dynamic random access memory, which is switch selectable between burst and pipelined modes." Applicant cannot find, and the Office has failed to show, a single instance where Manning discusses burst and pipelined modes together.

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the MPEP, and therefore, the rejection is improper. Reconsideration and allowance of claims 22-32 and 59 is respectfully requested.

Claims 60-61

The Office has failed to produce a *prima facie* case of anticipation. For example, claims 60-61 recite a multiplexer in combination with selection and temporary storage circuitry and control logic "for switching the memory circuit between a first mode of operation and a second

mode of operation." Applicant cannot find, and the Office has failed to show, this subject matter of claims 60-61 in Manning.

The Office indicated that the multiplexer can be found at Manning: Figure 1, mode register 40; Figure 5, multiplexer 66; multiplexed memory address at column 4, line 19; description of Figure 2 at column 8, lines 58+. These portions of Manning are insufficient to disclose the subject matter of claims 60-61. Applicant's multiplexer is for switching the memory circuit between a first mode of operation and a second mode of operation. Applicant cannot find where Manning discusses such multiplexer in mode register 40. The multiplexer 66 of Figure 5 is also used in Figure 3 of Manning. Figure 3 shows a write timing circuit designed to maximize the amount of time allowed for each write cycle to complete. See Manning at column 9, lines 45-46. Figure 5 is an alternate embodiment of Figure 3. Applicant cannot find where the multiplexer 66 of Manning switches a first mode of operation and a second mode of operation. It is unclear why the Office cited the multiplexed memory address at column 4, line 19. Applicant cannot find where at column 4, line 19, Manning discusses a multiplexer for switching between a first mode and a second mode. Figure 2 of Manning is a timing diagram for performing a burst read followed by a burst write. Applicant cannot find where Manning discusses the multiplexer as claimed in claims 60-61.

Because applicant cannot find and the Office fails to show the subject matter of claims 60-61, the rejection is improper and should be withdrawn. Reconsideration and allowance of claims 60-61 is respectfully requested.

Claims 63-65

The Office has failed to produce a *prima facie* case of anticipation. For example, claims 63-65 recite two multiplexers in combination with selection and temporary storage circuitry and control logic to operate in a pipelined mode. Applicant is unable to find, and the Office has failed to show, where Manning discusses this subject matter. The Office cited Manning at Figure 1, mode register 40; Figure 5, multiplexer 66; multiplexed memory address at column 4, line 19; Figure 1, counter 26; and description of Figure 2 at column 8, lines 58+. Applicant is unable to find the subject matter of claims 63-65 in these portions. Applicant in unable to understand how these cited portions work as the two multiplexers as claimed and described in the applicant's

specification. The Office also has failed to explain how these portions work. In fact, applicant cannot find where Manning discusses that these portions are used together as indicated by the Office. The counter 26 of Figure 1 of Manning is a counter--not a multiplexer. Applicant's discussion of other portions have been discussed above and are incorporated here in full.

In short, what is discussed by Manning is not identical to the subject matter of the present invention as required by the MPEP, and therefore, the rejection is improper. Reconsideration and allowance of claims 63-65 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 371-2129 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Commissioner of Patents, Washington, D.C. 20231 on **November 3, 2000**.

Tina Pugh
Name

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